NSWC PEBB Hardware Development Progress

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Topics To Be Covered

• PEBB High Power Hardware Refinement and Test Results
• PEBB Thermal Management
• PEBB Controller Refinement
PEBB High Power Hardware Refinement and Test Results
PEBB1.5 Hardware Refinement and Test Results

- 250kW Output Power Goal Reached
- Implemented and Planned Hardware Refinements
- Steps to Minimize ARCP Resonant Current
- Discussion of factors contributing to output voltage limitations
PEBB 1.5 ARCP Inverter

- Design Specifications: DC-AC operating mode
  - Input: 750 - 850Vdc
  - Output: 450Vac RMS at 250kW (water cooled)
- Major Components
  - Main switch - NonPunchThrough IGBT
  - Aux. Switch - Combo N-and P-MCT
  - DC Bus Caps - 6900 uF per phase
  - Resonant inductor - 1.0-1.2 uH
  - Resonant Cap - .2 uF/switch, .4uF/phase
  - DSP Based Digital Controller
    - 100ns step control of ac switch on time
    - at 800vdc = 40 amp step control
- Present status
  - Assembly completed 4/3/98
  - Tested up to 250kW 12/4/98
250kW Goal Reached

677Vdc Bus input
378Vac RMS output
382A RMS output

1.2uH Resonant Inductor
0.4uF Resonant Capacitor
5kHz Switching Frequency

410 kw on Load Bank, 1.2 µH and 0.4 µF
Implemented and Planned Hardware Refinements

- Shields around PEBB1.5 phase switch gate drives
  - devices turning on prior to zero voltage transition
  - bottom plate of laminated bus is positive bus
  - S1 gate drive referenced to phase-leg output which is switching from positive rail to negative rail
  - close proximity of S1 gate drive to positive bus suspected of causing false triggering through capacitive pickup
Implemented and Planned Hardware Refinements

- Shields around PEBB1.5 phase switch gate drives
Implemented and Planned Hardware Refinements

- Shields around PEBB1.5 phase switch gate drives
Implemented and Planned Hardware Refinements

• Gate drive operating mode
  - original design required sequential application of control turn-on signal followed by zero voltage transition
  - controller had 500ns deadtime to prevent shoot-through
  - high load current transitions approaching 500ns transitions
  - concern that transitions could arrive sooner than the turn-on signal
 Implemented and Planned Hardware Refinements

S2 Voltage vs Time (mS)

Resonant Current vs Voltage

Load Current
Implemented and Planned Hardware Refinements

• Gate drive operating mode
  - lowered deadtime to 300ns, added .2uf additional capacitance to lower dv/dt
  - proposed gate drive modification will change logic to an “AND” function with no sequential dependency
  - added hard switch enable signal to allow temporary hard switch transition for ARCP start-up
 Implemented and Planned Hardware Refinements

• Gate drive physical interface
  - eliminate PCMCIA connector - replace with connector with greater insertion depth and fewer pins
  - merge functions of gate drive and gate drive interface onto a single board
  - decrease input to output latency times while maintaining noise immunity
  - adaptable to existing PEBB1.5 as well as modified PEBB2 modules
Implemented and Planned Hardware Refinements

• Water jacket inlet and outlet modification
  - difficult to maintain watertight seal between brass fitting and plastic housing
  - plug existing holes and route water in and out through baseplate

• Power module modifications
  - changed terminal mounting nut thread size from 10-32 to 1/4-28 for improved handling of high current
Implemented and Planned Hardware Refinements
Steps to Minimize Resonant Current

PEBB 1.0 4/2/98 450 Volts DC with C Filter
Steps to Minimize Resonant Current
Projects to approximately 50A rms resonant current for...
Discussion of factors contributing to output voltage limitations
Discussion of factors contributing to output voltage limitations

• Possible Causes
  - Gate Drive Power Supply Voltage Isolation
  - Gate Drive Noise Pick-up
  - Phase Switch Diode Reverse Recovery
  - Thermal Sponge Integrity
PEBB Thermal Management
PEBB Thermal Management

- Functions of Existing PEBB Module Sponges
  - Thermal Transfer
  - Mechanical Support for Ceramic Base
  - Thermal Mass?
PEBB Thermal Management

- Short Comings of the Existing Copper Sponge
  - Variability of Thermal Performance
  - Degradation of Thermal Performance Due to Corrosion
  - Expensive and Complicated Manufacturing Process
PEBB Thermal Management

PEBB 1.5 Full Power Module
PEBB Thermal Management

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PEBB 1.5 Full Power Module
PEBB Thermal Management

PEBB 1.5 1/4 Power Module
PEBB Thermal Management
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PEBB Thermal Management
Measured Thermal Performance of PEBB 1.5 IGBT Module PH34 with Sponges and with a 0.030 in. Pin Manifold. Junction Temperatures Were Measured with the Sensor Mounted Internal to S2. (Note: These Resistance Values Cannot be Directly Compared to Those of the Instrumented Test Modules)
Measured Thermal Performance of PEBB 1.5 IGBT Modules with Both New and Used Sponges and with a 0.030 in. Pin Manifold. (Note: This Data is Based on a Sample of 2 New Modules and 1 Used Module)
Pressure Drop Vs. Flow for PEBB 1.5 Module with New Sponges and with 0.030 in. Pin Manifold.
Thermal Resistance Vs. Power Dissipation in S2 Using a Pin Manifold at 1.5 gpm Water Flow
PEBB Thermal Management

- Pin Manifold Advantages
  - Good, Predictable Thermal Performance
  - Free from Degradation (Only ceramic and plastic)
  - Easy and Inexpensive to Manufacture
  - Provides Mechanical Support for Ceramic Base (Not yet tested.)
PEBB Universal Controller

NSWC Annapolis
A Practical PEBB Vision
Existing ARCP Control

• Controls Auxiliary Circuit Ramp Time,
• Duty cycle is controlled indirectly \((D_{\text{actual}} = D_{\text{prog}} - BT1 - Tswg1 + BT2)\),
• Output node transition time is not fixed or measured.
• Open loop duty cycle compensation is used.
• Current feedback has significant latency.
Existing ARCP Control Implementation

\[ \text{Dmax} = T_s - BT1 - T1_{swg} - \text{AuxDelay2} \quad \text{(ideal)} \]

\[ \text{Dmax} = T_s - BT1_{max} - T1_{swg \text{Max}} - \text{AuxDelayConstant} - \text{DutyCompMax} - \text{TotalMargin} \]

\[ = T_s - (3.0 + 2.0 + 4.8 + 3.0 + 7.2) \]

\[ = T_s - 20\text{usec} \]
Resonant Cap  0.2 uF
Resonant Cap
0.4 uf
Existing ARCP Control Implementation

Dmax = Ts - BT1 - T1swg - AuxDelay2 (ideal)

Note:
The Total Margin is what is currently employed in the NSWC PEBB 1.5. This could be reduced to 2.2 usec. We will assume the optimistic loss of only 15usec for the comparison with the smart gate drive control.

450VAC @ 20 kHz would require an estimated 1600 VDC!!
Existing ARCP Control Implementation

• 450 VAC obtainable from 800 VDC @ 5kHz
• Existing PEBB 1.5 Total Safety Margin = 7.2us
  - The Safety Margin could be theoretically reduced to 2.2us, this results in a total loss of 15us and it is this number that will be used in the comparison with the smart gate drive implementation.
• At 20 kHz over 1600 VDC would be required to obtain 450 VAC
IDEAL Voltage Gain

\[
V_{L-L} = \frac{\sqrt{3}}{2\sqrt{2}} \left[ V_{DC} \frac{2D_{MAX}}{1} \right] \frac{2}{\sqrt{3}}
\]

Note: Third harmonic inserted.
ARCP Smart Gate Drive Control

Dmax = Ts - BT1 - T1swg - AuxDelay2 (ideal)

DutyMax = Ts - BT1@Dmax - T1swg@Dmax - AuxDelay2@Dmax - ActiveMargin

= Ts - (1.8 + 0.8 + 2.0 + 1.0)

= Ts - 5.6usec
ARCP Smart Gate Drive Control

• Duty Cycle Directly Controlled
  - Improved Power Quality

• Dramatic Increase in DC Bus Utilization
  - 450 VAC @ 20 kHz requires an estimated 825 VDC

• Guarantees Correct Converter State Progression

• Provides Additional Hardware Protection

• Allows Performance to be Safely Maximized
ARCP PEBB Power Quality

- Existing control has indirect control of the duty cycle and inherent data latencies limiting achievable power quality.
- Direct control of the Duty is desirable. The duty cycle must not be allowed to dither.
- This requires the Bus Transition Times to be known by the hardware controller.
PEBB STD Control Interface

• Smart Gate Drives and a Hardware Manager allows the encapsulation of all hardware specific knowledge within the PEBB and outside of the PEBB Controller.

• A standard interface between the PEBB Universal Controller and the PEBB can consist of an analog port and a digital communication port.
ARCP Smart Gate Drives

Diagram:
- PEBB Universal controller
- Hardware Manager
  - Main Gate Drives
  - Aux Gate Drives
- PEBB Power Block
  - PEBB STD interface
Communicates to the Topology Independent Output

PEBB Universal Controller
Topology Independent Output
Communicates to the Hardware
Manager via Digital Interface

Hardware Topology Specific

A
B
C
ARCP Smart Gate Drives

- Use embedded FPGA as Hardware Manager
- Control the duty cycle directly.
- Zero voltage detection for main device.
- Measure output node transition.
- Zero current turn-off of auxiliary circuit.
PEBB Hardware Manager

• Responsible for the operation and safety of the hardware. Achieves maximum performance.
• Receives desired duty cycle data from digital port.
• Utilizes Smart Gate Drives and Current Feedback.
• Based on FPGA technology.
Digital Communications Port

- Allows flexible and expandable systems.
- The Northrup Grumman PEBB controllers have a 16bit wide expansion bus.
- IEEE 1394 with +100Mb/s throughput is a serial link that uses 125us time slices. It is well suited for switching frequencies below 8 kHz. However, realizable bandwidth for small packets at 20 kHz is an open question.
PEBB Universal Controller (PUC)

- Independent of Power Circuit Topology. Calculate duty cycle for each phase leg.
- Communicates to the PEBB Hardware Manager digitally.
- Receives analog signals from PEBB for closed loop control.
- Receives Global Communications. (Type?)
- Encapsulation of hardware specific information allows the Controller itself to be partitioned.
All control algorithms are Independent of Topology. e.g. An ARCP PEBB could use the exact control algorithm as a Hard switched PEBB.

Encapsulation of hardware specific information allows the PUC itself to be partitioned.

The algorithm can be independent of the controller.

The same Algorithm could be run on various PEBB controllers.
PEBB Control Algorithm Programming

• Algorithms are partitioned from the controller hardware utilizing encapsulation techniques.
• Algorithms are Power Topology Independent.
• Algorithms are programmed in C or C++.
• Commercial GUI code generators (Simulink) could be utilized directly.
PEBB Control Dreaming?

• This all sounds great.... but a bit to lofty right?
• Not with proper choices now!
• Demonstrable at PCIM 99.